CLAIMS

What is claimed is:

1. A system comprising:

a memory, wherein the memory includes a plurality of logical memory devices; and

a network switch coupled to the memory, wherein the switch is adaptable to write a first portion of received packet data to a first of the plurality of logical memory devices and to write a second portion of the packet data to a second of the plurality of logical memory devices.

2. The system of claim 1 wherein the network switch is further adaptable to write a third portion of received packet data to a third of the plurality of logical memory devices.

3. The system of claim 1 wherein the network switch comprises a memory controller.

4. The system of claim 3 wherein the memory controller comprises:

a first memory controller component coupled to the first logical memory device; and

a second memory controller component coupled to the second logical memory device.

5. The system of claim 4 wherein the first memory controller component and the second memory controller component access the corresponding logical memory devices via a shared address line.

6. The system of claim 2 wherein the first, second and third logical memory devices comprise synchronous dynamic random access memories (SDRAMs).

7. The system of claim 2 wherein the first logical memory devices comprises a synchronous static random access memories (SSRAMs) and the second and third logical memory devices comprise synchronous dynamic random access memories (SDRAMs).

8. The system of claim 3 wherein the memory controller maintains a record of the last of the plurality of logical memory devices that was written to.

9. The system of claim 3 wherein the network switch further comprises:

a receiver coupled to the memory controller;

a transmitter coupled to the memory controller;

address resolution logic coupled to the memory controller; and

packet queuing control coupled to the memory controller, the receiver, the transmitter and the address resolution logic.

10. The system of claim 3 wherein the network switch further comprises a media access controller (MAC) coupled to the receiver, wherein the MAC receives packet data via a plurality of ports coupled to the receiver.

11. A network switch comprising:

a first media access controller (MAC) coupled to a plurality of ports;

a receiver coupled to the first MAC; and

a memory controller coupled to the receiver, wherein the memory controller is adaptable to write a first portion of a first data packet received from a first of the plurality of ports to a first logical memory device and write a second portion of the first data packet received from the first port to a second logical memory device.

12. The system of claim 11 wherein the memory controller is further adaptable to write a third portion of the first data packet received from the first port to a third logical memory device.

13. The system of claim 11 wherein the memory controller is adaptable to write a first portion of a second data packet received from the first port to a third logical memory device and write a second portion of the second data packet received from the first port to a fourth logical memory device.

14. The system of claim 11 wherein the memory controller is adaptable to write a first portion of a first data packet received from a second of the plurality of ports to the first logical memory device and write a second portion of the first data packet received from the second port to a second logical memory device.

15. The system of claim 11 wherein the memory controller comprises:

a first memory controller component coupled to the first logical memory device; and

a second memory controller component coupled to the second logical memory device.

16. The system of claim 15 wherein the first memory controller component and the second memory controller component access the corresponding logical memory devices via a shared address line.

17. The system of claim 12 wherein the first, second and third logical memory devices comprise synchronous dynamic random access memories (SDRAMs).

18. The system of claim 12 wherein the first logical memory devices comprises a synchronous static random access memories (SSRAMs) and the second and third logical memory devices comprise synchronous dynamic random access memories (SDRAMs).

19. A method comprising:

receiving a first data packet at a network switch;

writing a first portion of the first data packet to a first logical memory device coupled to the network switch; and

writing a second portion of the first data packet to a second logical memory device coupled to the network switch.

20. The method of claim 19 further comprising writing a third portion of the first data packet to a third logical memory device coupled to the network switch.

21. The method of claim 19 further comprising:

receiving a second data packet at a network switch;

writing a first portion of the second data packet to the first logical memory device; and

writing a second portion of the second data packet to the second logical memory device.

22. The method of claim 19 further comprising determining at the network switch the last logical memory device to which a portion of the first data packet was written.

23. The method of claim 22 further comprising:

determining whether the size of a third portion of the first data packet is less than a predetermined value; and

if so, writing the third portion of the second data packet to both banks of a third logical memory device.

24. The method of claim 22 further comprising:

determining whether the size of a third portion of the first data packet is less than a predetermined value; and

if not, writing a first sub-portion of the third portion of the first data packet to a first bank of a third logical memory device and writing a second sub-portion of the third portion of the first data packet to a second bank of the third logical memory device.